Appl. No. 09/654,115

Amendments to the Claims:

  This listing of claims will replace all prior versions, and listings, of claims in the application. The claims are as follows:

Listing of Claims:

  1. (Original) A computer system having cache circuitry, the computer system adapted to be controlled by a computer program to cache information, comprising:

  cache circuitry, including a cache memory adapted to store information related to a computer program;

  a main memory adapted to store the information;

  a processor adapted to be controlled by the computer program and adapted to cooperate with a bus interface unit to direct selected portions of the information to the cache circuitry based at least in part on cacheability determinations made during compilation of the computer program; and

  bus circuitry, operatively connecting the processor, the cache circuitry, and the main memory.

  2. (Original) The system of claim 1, wherein the information comprises instructions of the computer program.

  3. (Original) The system of claim 1, wherein the information comprises data accessed by the computer program.

  4. (Original) The system of claim 1, wherein the selected portions are marked by a compiler during the compilation of the computer program such that the bus interface unit can identify the selected portions during execution of the computer program.

Appl. No. 09/654,115

5.   (Original) The system of claim 1, wherein each piece of the information contains marking bits, and a compiler sets the marking bits of the selected portions of the information during the compilation of the computer program.

6.   (Original) The system of claim 1, wherein the compilation of the computer program comprises translating a source code of the computer program to an object code.

7.   (Original) The system of claim 1, wherein the compilation of the computer program comprises programming an object code for the computer program directly.

8.   (Original) The system of claim 1, wherein the cacheability determinations comprise determinations that the selected portions are cacheable.

9.   (Original) The system of claim 1, wherein the cache circuitry includes at least a first cache memory and a second cache memory, and wherein the cacheability determinations comprise determinations as to whether to cache each of the selected portions in the first or second cache memory.

10.   (Original) The system of claim 9, wherein the first cache is a level-one cache and the second cache is a level-two cache.

11.   (Original) The system of claim 1, wherein the cache circuitry supports both write-back and write-through caching methods, and the cacheability determinations comprise determinations whether each of the selected portions is cacheable using the write-back or write-through caching method.

12.   (Original) The system of claim 1, wherein the cache circuitry includes at least one N-way associative cache, wherein N is a number greater than one.

Appl. No. 09/654,115

13.   (Original) The system of claim 1, further comprising a compiler adapted to optimize the cacheability determinations.

14.   (Original) The system of claim 13, wherein the compiler is adapted to optimize the cacheability determination for a first piece of the information based at least in part on whether caching of the first piece of information is likely to cause thrashing of the cache circuitry.

15.   (Original) The system of claim 13, wherein the cache circuitry employs a cache-management scheme, and wherein the compiler is adapted to optimize the cacheability determination for a first piece of the information based at least in part on the cache-management scheme.

16.   (Original) The system of claim 15, wherein the cache management scheme comprises the level of associativity of the cache memory.

17.   (Original) The system of claim 13, wherein the compiler is adapted to optimize the cacheability determination for a first piece of the information based at least in part on the likely frequency that the first piece of information will be accessed by the processor during execution of the computer program.

18.   (Original) The system of claim 13, wherein the compiler is adapted to optimize the cacheability determination for a first piece of the information based at least in part on what other piece of the information is likely to be overwritten in the cache circuitry if the first piece of information is cached.

19.   (Original) The system of claim 13, wherein the cacheability determinations are accomplished during the compilation of a program code into an object code by utilizing profile-based optimizations.

Appl. No. 09/654,115

20.   (Original) The system of claim 1, wherein the system further comprises a system controller, adapted to retrieve and send instructions and data to the main memory via the bus circuitry.

21.   (Original) The system of claim 1, wherein the system further comprises at least one bus device connecting an external storage device to the bus circuitry.

22.   (Original) The system of claim 21, wherein the external storage device provides instructions utilized by the processor in performing a desired task, the instructions being optimized for cacheability.

23.   (Original) The system of claim 22, wherein the instructions are compiled by a compiler adapted to optimize cacheability determinations.

24.   (Original) The system of claim 1, wherein the cache circuitry and the processor are provided on a single chip.

25.   (Original) A system for determining which portions of a program code to cache and which to not cache, comprising:
        a memory device containing a program code; and
        a processor connected to the memory device, the processor being adapted to be controlled by the program code to direct selected portions of the program code to a cache based at least in part on cacheability determinations made during compilation of a computer program.

26.   (Original) The system of claim 25, wherein the program code includes instructions.

27.   (Original) The system of claim 25, wherein the program codes includes data.

Appl. No. 09/654,115

28.   (Original) The system of claim 25, wherein each of the selected portions of the program code contains at least one marking bit designating the selected portion as suitable for caching, the marking bit being set by a compiler during compilation of the computer program.

29.   (Original) The system of claim 25, the processor is connected to the memory device via bus circuitry.

30.   (Original) The system of claim 25, wherein the processor further comprises a level one cache.

31.   (Original) The system of claim 30, wherein the system further comprises a level two cache connected to the processor and the memory device via a bus circuitry.

32.   (Original) The system of claim 25, wherein the memory device further comprises a main memory for a computer system.

33.   (Original) The system of claim 25, wherein the memory device further comprises an external storage device connected to and accessible by the processor via a bus circuitry.

34.   (Original) A method for controlling the cacheability of information in a computer system, comprising:

compiling a computer program, by:

making cacheability determinations for information associated with the computer program; and

marking at least selected portions of the information according to the determinations;

Page 6 of 16

Appl. No. 09/654,115

executing the computer program on a computer system, the computer system including cache circuitry;

detecting the marking of the selected portions of the information during execution of the computer program; and

directing the selected portions of the information to the cache circuitry according to the marking.

35.   (Original) The method of claim 34, wherein the information comprises instructions of the computer program.

36.   (Original) The method of claim 34, wherein the information comprises data to be accessed by the computer program.

37.   (Original) The method of claim 34, wherein each piece of the information contains marking bits and the act of marking includes setting the marking bits of at least the selected portions of the information.

38.   (Original) The method of claim 34, wherein the step of compiling comprises translating a source code of the computer program to an object code.

39.   (Original) The method of claim 34, wherein the step of compiling comprises programming an object code for the computer program directly.

40.   (Original) The method of claim 34, wherein the act of making cacheability determinations comprises determining that the selected portions are cacheable.

41.   (Original) The method of claim 34, wherein the cache circuitry comprises a first cache memory and a second cache memory and wherein the act of making cacheability determinations comprises determining whether to cache each of the selected portions in the first cache memory or the second cache memory.

42.   (Original) The method of claim 34, wherein the cache circuitry supports both write-back and write-through caching methods, and the act of making cacheability determinations comprises determining whether to cache each of the selected portions using the write-back or write-through caching method.

43.   (Original) The method of claim 34, wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on whether the caching the first piece of information is likely to cause thrashing of the cache circuitry.

44.   (Original) The method of claim 34, wherein the cache circuitry employs a cache-management scheme, and wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on the cache-management scheme.

45.   (Previously presented) The method of claims 34, wherein the cache circuitry includes at least a first cache memory, and wherein the act of making cacheability determinations for information associated with the computer program comprises making cacheability determinations based on the level of associativity of the first cache memory.

46.   (Original) The method of claim 34, wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on the likely frequency that the first piece of information will be accessed by the processor during execution of the computer program.

47.   (Original) The method of claim 34, wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on what other piece of the information is likely to be overwritten in the cache circuitry if the first piece of information is cached.

Appl. No. 09/654,115

48.   (Original) A method for compiling a computer program, comprising:

making cacheability determinations for information associated with the computer program; and

marking at least selected portions of the information according to the determinations.

49.   (Original) The method of claim 48, wherein the information comprises instructions of the computer program.

50.   (Original) The method of claim 48, wherein the information comprises data to be accessed by the computer program.

51.   (Original) The method of claim 48, wherein each piece of the information contains marking bits and the act of marking includes setting the marking bits of at least the selected portions of the information.

52.   (Original) The method of claim 48, further comprising translating a source code of the computer program to an object code.

53.   (Original) The method of claim 48, further comprising programming an object code for the computer program directly.

54.   (Original) The method of claim 48, wherein the act of making cacheability determinations comprises determining that the selected portions are cacheable.

55.   (Original) The method of claim 48, wherein the act of making cacheability determinations comprises determining whether to cache each of the selected portions in a first cache memory or a second cache memory.

Appl. No. 09/654,115

56.   (Original) The method of claim 48, wherein the act of making cacheability determinations comprises determining whether to cache each of the selected portions using a write-back or a write-through caching method.

57.   (Original) The method of claim 48, wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on whether the caching the first piece of information is likely to cause thrashing of the cache circuitry.

58.   (Original) The method of claim 48, wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on a cache-management scheme.

59.   (Original) The method of claim 58, wherein the cache management scheme comprises the level of associativity of a cache memory,

60.   (Original) The method of claim 48, wherein the act of making cacheability determinations includes making a cacheability determination for a first piece of the information based at least in part on the likely frequency that the first piece of information will be accessed by a processor during execution of the computer program.

61.   (Original) The method of claim 48, wherein the act of making cacheability determinations comprises making a cacheability determination for a first piece of the information based at least in part on what other piece of the information is likely to be overwritten in a cache circuitry if the first piece of information is cached.